## AMENDMENTS TO THE CLAIMS

1. (Original) A processor, comprising:

circuit to receive a macro instruction specifying an operation, and specifying a first and a second data operand in first and second registers, respectively; and

one or more execution units to split the macro instruction into a first micro instruction and a second micro instruction, the first micro instruction specifying the operation on a first corresponding segment including a first portion of the first data operand and a first portion of the second data operand, and the second micro instruction specifying the operation on a second corresponding segment including a second portion of the first data operand and a second portion of the second data operand, and to execute the first micro instruction, and to execute the second micro instruction.

2. (Original) The processor of claim 1, wherein the execution of the first micro instruction is performed during a first clock cycle.

3. (Original) The processor of claim 1, wherein the execution of the second micro instruction is performed during a subsequent clock cycle.

4. (Original) The processor of claim 1, wherein the execution of the first micro instruction is performed during a first half clock cycle.

5. (Original) The processor of claim 1, wherein the execution of the second micro instruction is performed during a second half clock cycle.

6. (Original) The processor of claim 1, further comprises a register file coupled with the circuit, the register file having a third data operand including a plurality of data elements corresponding to the first data operand and the second data operand.

7. (Original) The processor of claim 6, wherein the plurality of data elements includes 128-bits of data from the register file.

8. (Original) A system, comprising:

a storage medium;

a processor coupled with the storage medium, the processor having

circuit to receive a macro instruction specifying an operation, and specifying a first and a second data operand in first and second registers, respectively, and

one or more execution units to split the macro instruction into a first micro instruction and a second micro instruction, the first micro instruction specifying the operation on a first corresponding segment including a first portion of the first data operand and a first portion of the second data operand, and the second micro instruction specifying the operation on a second corresponding segment including a second portion of the first data operand and a second portion of the second data operand, and to execute the first micro instruction, and to execute the second micro instruction; and

a register file coupled with the processor, the register file having a third data operand including a plurality of data elements corresponding to the first data operand and the second data operand.

9. (Original) The system of claim 8, wherein the execution of the first micro instruction is performed during a first clock cycle, and the execution of the second micro instruction is performed during a second clock cycle.

10. (Original) The system of claim 8, wherein the execution of the first micro instruction is performed during a first half clock cycle, and execution of the second micro instruction is performed during a second half clock cycle.

11. (Original) A method, comprising:

receiving a macro instruction specifying an operation, and specifying a first and a second data operand in first and second registers, respectively; and

splitting the macro instruction into a first micro instruction and a second micro instruction, the first micro instruction specifying the operation on a first corresponding segment including a first portion of the first data operand and a first portion of the second data operand, and the second micro instruction specifying the operation on a second corresponding segment including a second portion of the first data operand and a second portion of the second data operand.

12. (Original) The method of claim 11, further comprising:

executing the first micro instruction; and

executing the second micro instruction.

13. (Original) The method of claim 12, wherein the execution of the first micro instruction is performed during a first clock cycle, and the execution of the second micro instruction is performed during a second clock cycle.

14. (Original) The method of claim 13, wherein the execution of the first micro instruction is performed during a first clock cycle, and the execution of the second micro instruction is performed during a second clock cycle.

15. (New) A method, comprising:

receiving a macro instruction specifying an operation, and specifying first and second data operands in first and second registers, respectively;

performing the operation on lower order data segments of the first and second data operands on a first set of execution units; and

performing the operation on high order data segments of the first and second data operands on the first set of execution units.

16. (New) The method of claim 15, further comprises splitting the macro instruction into a first micro instruction and a second micro instruction.

17. (New) The method of claim 16, wherein the first micro instruction specifying the operation on a first corresponding segment including a first portion of the first data operand and a first portion of the second data operand.

18. (New) The method of claim 16, wherein the second micro instruction specifying the operation on a second corresponding segment including a second portion of the first data operand and a second portion of the second data operand.

19. (New) The method of claim 16, further comprising:

executing the first micro instruction; and

executing the second micro instruction.

20. (New) A method, comprising:

receiving a first macro instruction specifying a first operation, and specifying first and second data operands in first and second registers, respectively;

receiving a second macro instruction specifying a second operation, and specifying the first and the second data operands in the first and second registers, respectively;

at time T, performing the first operation on lower order data segments of the first and second data operands on a first set of execution units;

at time T+1, performing the first operation on high order data segments of the first and second data operands on the first set of execution units;

at time T+2, performing the second operation on lower order data segments of the first and second data operands on the first set of execution units; and

at time T+3, performing the second operation on high order data segments of the first and second data operands on the first set of execution units.

21. (New) The method of claim 20, further comprises splitting the macro instruction into a first micro instruction and a second micro instruction.

22. (New) The method of claim 21, wherein the first micro instruction specifying the operation on a first corresponding segment including a first portion of the first data operand and a first portion of the second data operand.

23. (New) The method of claim 21, wherein the second micro instruction specifying the operation on a second corresponding segment including a second portion of the first data operand and a second portion of the second data operand.

24. (New) The method of claim 21, further comprising:

executing the first micro instruction; and

executing the second micro instruction.

25. (New) A processor, comprising:

circuit to receive a macro instruction specifying an operation, and specifying first and second data operands in first and second registers, respectively; and

an execution unit in communication with the circuit, the execution unit to perform the operation on lower order data segments of the first and second data operands on a first set of execution units, and to perform the operation on high order data segments of the first and second data operands on the first set of execution units.

26. (New) The processor of claim 25, wherein the execution unit is further to split the macro instruction into a first micro instruction and a second micro instruction.

27. (New) The processor of claim 26, wherein the first micro instruction specifying the operation on a first corresponding segment including a first portion of the first data operand and a first portion of the second data operand.

28. (New) The processor of claim 26, wherein the second micro instruction specifying the operation on a second corresponding segment including a second portion of the first data operand and a second portion of the second data operand.

29. (New) The processor of claim 26, wherein the execution unit is further to:

execute the first micro instruction; and

execute the second micro instruction.

30. (New) A system, comprising:

a storage medium;

a processor coupled with the storage medium, the processor having

circuit to receive a macro instruction specifying an operation, and specifying first and second data operands in first and second registers, respectively;

an execution unit in communication with the circuit, the execution unit to perform the operation on lower order data segments of the first and second data operands on a first set of execution units, and to perform the operation on high order data segments of the first and second data operands on the first set of execution units; and

a register file coupled with the processor, the register file having a third data operand including a plurality of data elements corresponding to the first data operand and the second data operand.

31. (New) The system of claim 30, wherein the execution unit is further to split the macro instruction into a first micro instruction and a second micro instruction.

32. (New) The system of claim 31, wherein the first micro instruction specifying the operation on a first corresponding segment including a first portion of the first data operand and a first portion of the second data operand.

33. (New) The system of claim 31, wherein the second micro instruction specifying the operation on a second corresponding segment including a second portion of the first data operand and a second portion of the second data operand.

34. (New) The system of claim 31, wherein the execution unit is further to:

execute the first micro instruction; and

execute the second micro instruction.

35. (New) A machine-readable medium having stored thereon data representing sets of instructions which, when executed by a machine, cause the machine to:

receive a macro instruction specifying an operation, and specifying first and second data operands in first and second registers, respectively;

perform the operation on lower order data segments of the first and second data operands on a first set of execution units; and

perform the operation on high order data segments of the first and second data operands on the first set of execution units.

36. (New) The machine-readable medium of claim 35, wherein the sets of instructions which, when executed by the machine, further cause the machine to split the macro instruction into a first micro instruction and a second micro instruction.

37. (New) The machine-readable medium of claim 36, wherein the first micro instruction specifying the operation on a first corresponding segment including a first portion of the first data operand and a first portion of the second data operand.

38. (New) The machine-readable medium of claim 36, wherein the second micro instruction specifying the operation on a second corresponding segment including a second portion of the first data operand and a second portion of the second data operand.

39. (New) The machine-readable medium of claim 36, wherein the sets of instructions which, when executed by the machine, further cause the machine to:

execute the first micro instruction; and

execute the second micro instruction.

40. (New) A machine-readable medium having stored thereon data representing sets of instructions which, when executed by a machine, cause the machine to:

receive a first macro instruction specifying a first operation, and specifying first and second data operands in first and second registers, respectively;

receive a second macro instruction specifying a second operation, and specifying the first and the second data operands in the first and second registers, respectively;

at time T, perform the first operation on lower order data segments of the first and second data operands on a first set of execution units;

at time T+1, perform the first operation on high order data segments of the first and second data operands on the first set of execution units;

at time T+2, perform the second operation on lower order data segments of the first and second data operands on the first set of execution units; and

at time T+3, perform the second operation on high order data segments of the first and second data operands on the first set of execution units.

41. (New) The machine-readable medium of claim 40, wherein the sets of instructions which, when executed by the machine, further cause the machine to split the macro instruction into a first micro instruction and a second micro instruction.

42. (New) The machine-readable medium of claim 41, wherein the first micro instruction specifying the operation on a first corresponding segment including a first portion of the first data operand and a first portion of the second data operand.

43. (New) The machine-readable medium of claim 41, wherein the second micro instruction specifying the operation on a second corresponding segment including a second portion of the first data operand and a second portion of the second data operand.

44. (New) The machine-readable medium of claim 41, wherein the sets of instructions

which, when executed by the machine, further cause the machine to:

execute the first micro instruction; and

execute the second micro instruction.